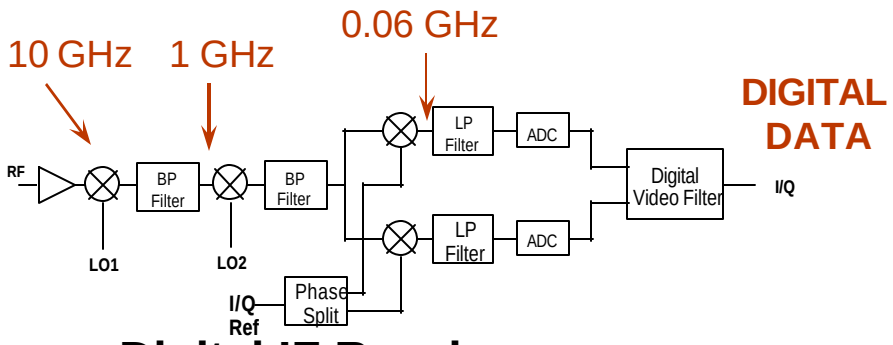
Continuous-Time $\Delta\Sigma$ Modulators for RF Applications

April 14 2005

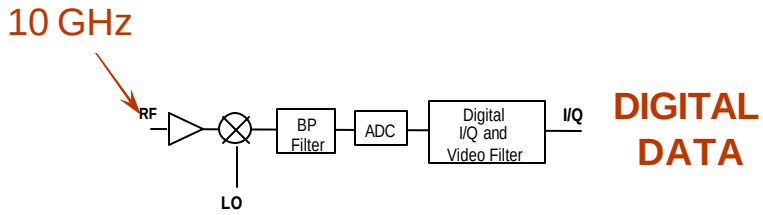
Joe Jensen
Todd Kaplan
HRL Laboratories, LLC

ADCs in Digital Receivers: Towards the "Software Radio"

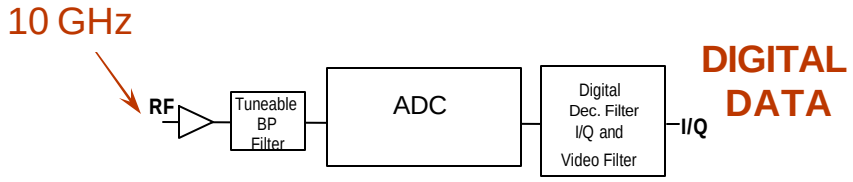
Conventional Receiver



Digital IF Receiver



Digital RF Receiver



Trend - Eliminate Downconversion

Advantages:

- Digital robustness
- frequency agility
- Lower I/Q Images
- Better Channel Match
- Flexibility with communication standards
- More Deg of Freedom

Challenges:

- ADC needs enormous dynamic range
- Enormous data reduction needed in DSP

Joe Jensen
(310) 317-5250
jfjensen@hrl.com

Issues in Moving ADC forward in Signal Path in Digital Receivers

- High ADC sample rates required
  - High input bandwidth and fast settling needed for sub-sampling approaches
  - Direct sampling requires higher sample rate than the IF or RF being sampled
- High ADC dynamic range required
  - Interfering signals in digital receiver are blocked after the ADC
  - Additional ADC dynamic range is need to replace blocking filters and AGC functions
- ADC limitations
  - Increasing the sample rate of ADCs decreases the ADC dynamic range
  - Digital receiver requirements stress ADC fundamental limits

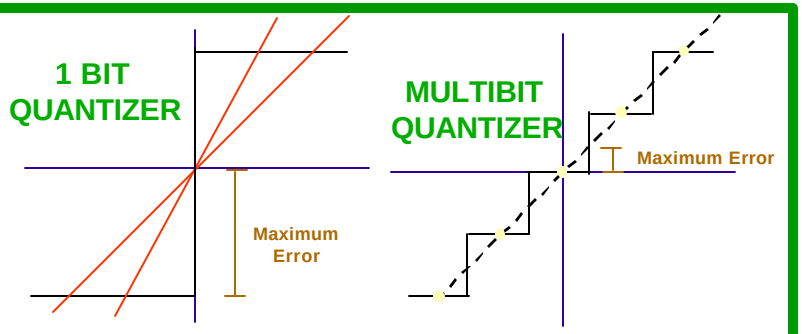
Ultra-Fast IC technology will have a major impact on Digital Receiver Technology

Joe Jensen
(310) 317-5250
jfjensen@hrl.com

Fundamental Principles Oversampling

Linearity:

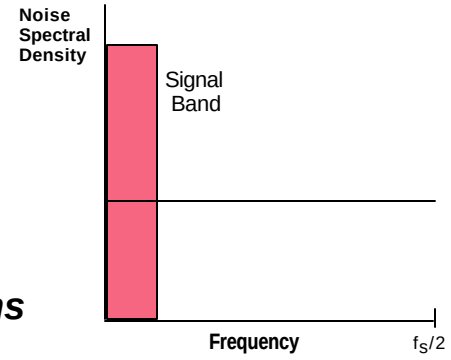
- Linearity of multibit quantizer determined by accuracy of voltage thresholds (process uniformity)
- 1 - Bit quantizer (= Comparator)
  - Inherently linear
- 1-Bit quantizer increases quantization noise



Resolution:

Oversampling (= Averaging)

- Improves Resolution @ 3 dB / Octave
- Requires High Speed Technology



Very High Oversampling Required for Practical Applications

- 10 bit, 50 MHz Requires Comparator Clocked @ 12.5 THz !!

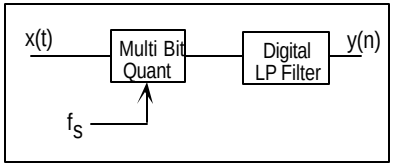
Practical Realization : Add loop filter to shape noise and improve performance.

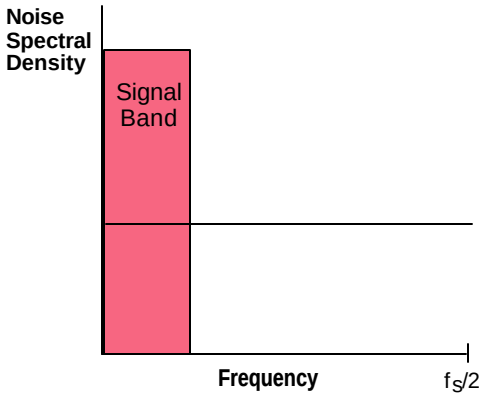
Joe Jensen
(310) 317-5250
jfjensen@hrl.com

slide #4

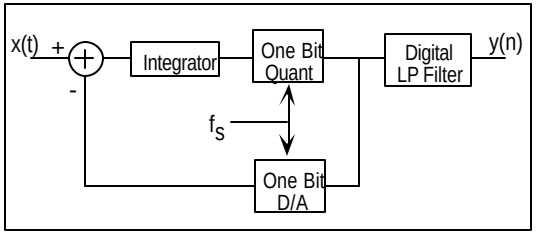
Bandpass DS Noise Shaping for Digital Receiver Applications

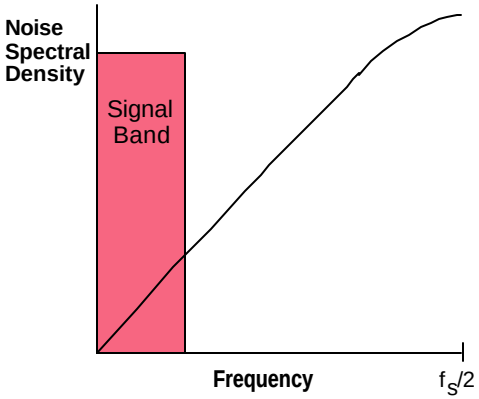
Conventional Oversampling ADC



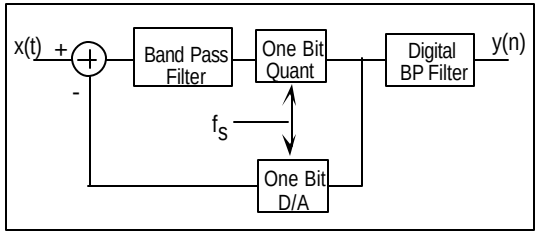


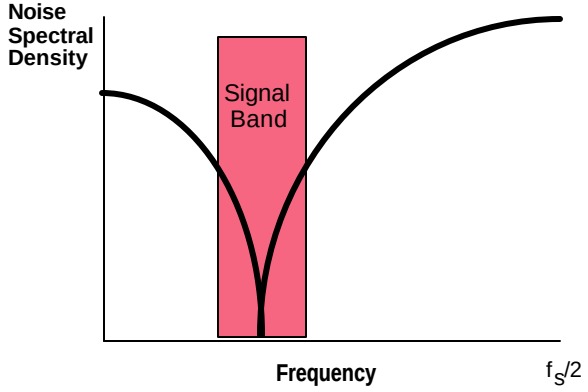
Delta-Sigma Oversampling ADC





Bandpass Delta-Sigma ADC



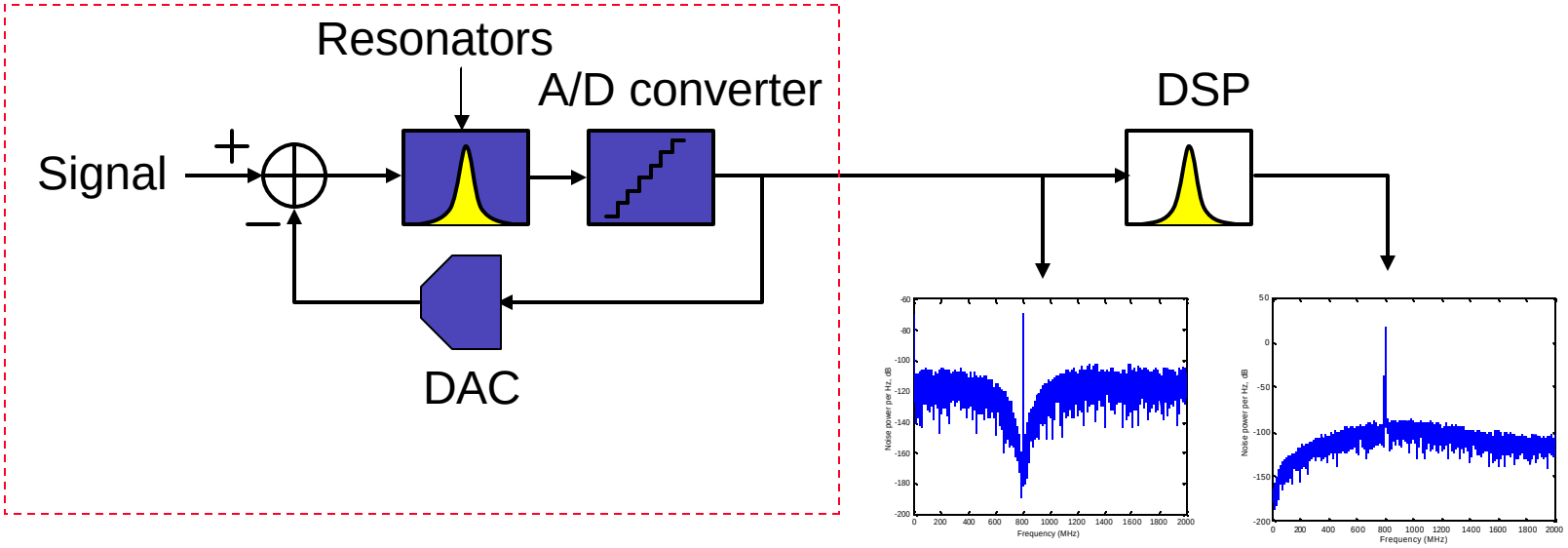


The Noise Suppression Region Can Be "Tuned" Away From DC By Replacing The Lowpass Filter With A Bandpass Filter

Joe Jensen
(310) 317-5250
jfjensen@hrl.com

slide #5

Principle of bandpass DS modulation



ΔΣ modulator

Digitized output

- **A/D converter is put inside a feedback loop**
- **Quantizer error is reduced by the gain of the feedback loop**

Advantages: Unmatched resolution for high-IF digitization

Disadvantages: The DAC and input resonator still require full dynamic range of final desired output

Continuous Time DS vs. Discrete Time DS

- **Clock rate**
  - **SC DT DSM maximum clock rate is limited by op amp bandwidth**
    - **maximum clock rate ~ f_T/100**
  - **CT DSM relax the restriction on op amp bandwidth**
    - **maximum clock rate ~ f_T/20**
- **Switching Transients**
  - **SC DT DSM have larger switching transients than CT DSM**
- **Aliasing**
  - **SC DT DSM require separate filter at their inputs to attenuate aliases sufficiently**
  - **CT DSM have free anti-aliasing**
    - **antialiasing is an inherent property of the mathematics of CT DSM**

Design Approach for Continuous Time Modulators

Available Devices in High Speed Bipolar Technology

- **NPN transistors**
- **Resistors: Thin Film 50Ω /sq, Base Epi 800 Ω/sq**
- **Capacitors: Metal-Insulator-Metal**

Consequences

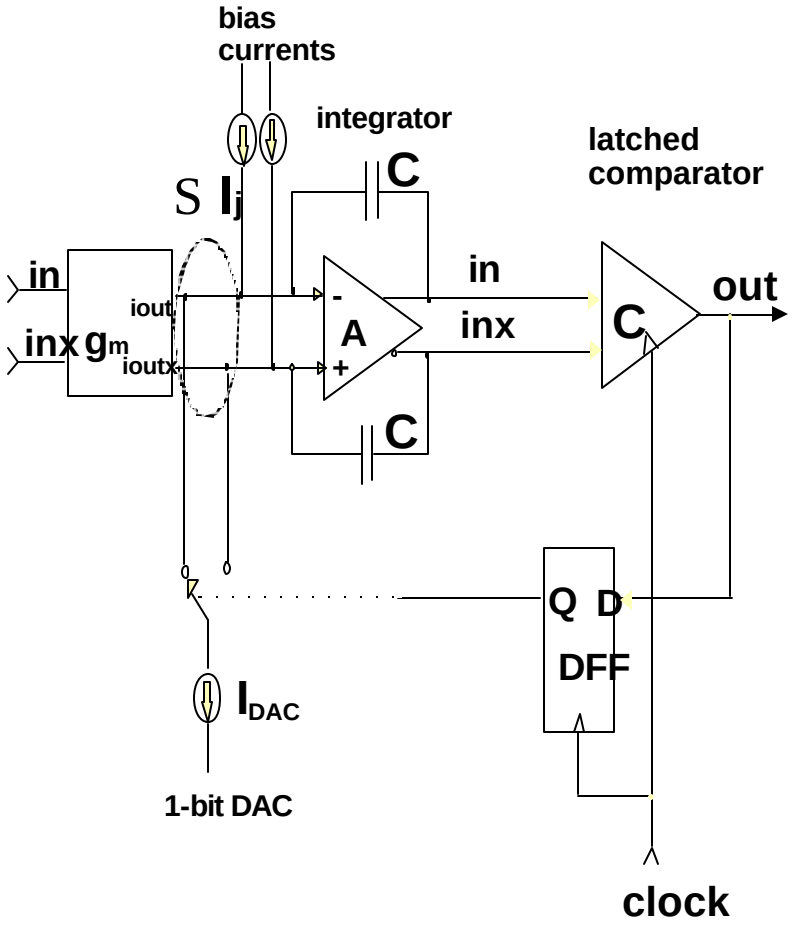
- **Low OpAmp Voltage Gain (typ < 100)**
- **No Simple Positive Current Sources or Active Loads**
- **No Switched Capacitors**

Design Approach

- **Continuous Time Integrators**
- **Transimpedance Amplifiers**
- **Fully Differential Circuitry to Minimize Noise Coupling**
- **Current-Mode Logic Minimizes Switching Noise**

InP HBT ΔΣ Modulator Implementation

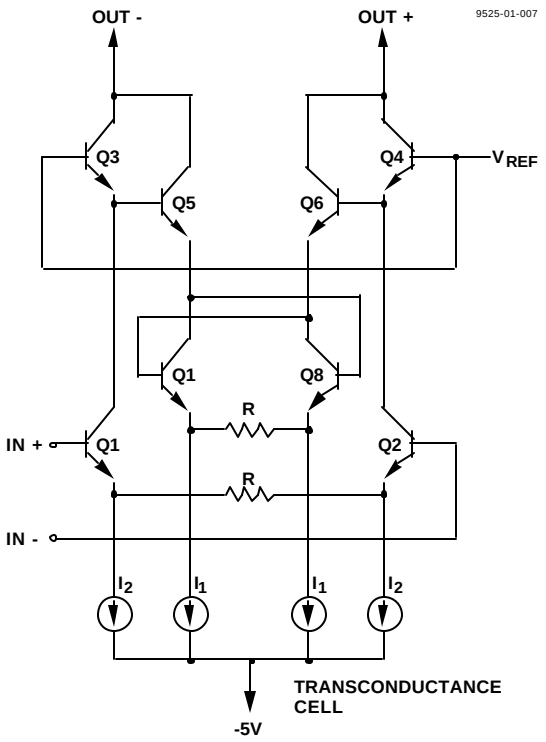
1st Order Low Pass ΔΣ Modulator

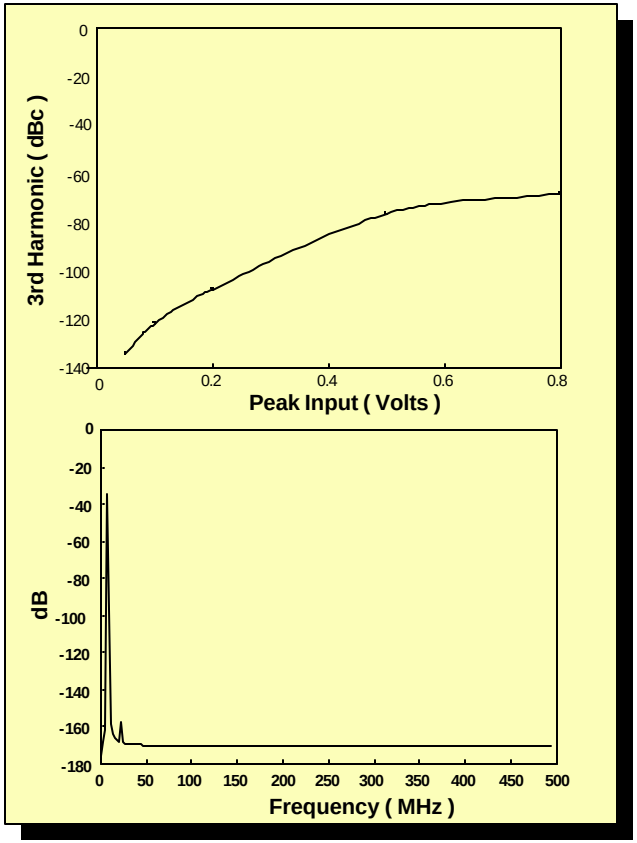


- **Basic Approach: High impedance current drive in a feedback integrator**
  - **Tolerant of low amplifier gain**
  - **Low voltage swing at input to integrating capacitors minimizes integrator leakage**
  - **Allows current-summing for dac summing node**
  - **Requires positive bias current source**
- **Input transconductance cell outside feedback loop-determines overall circuit linearity**

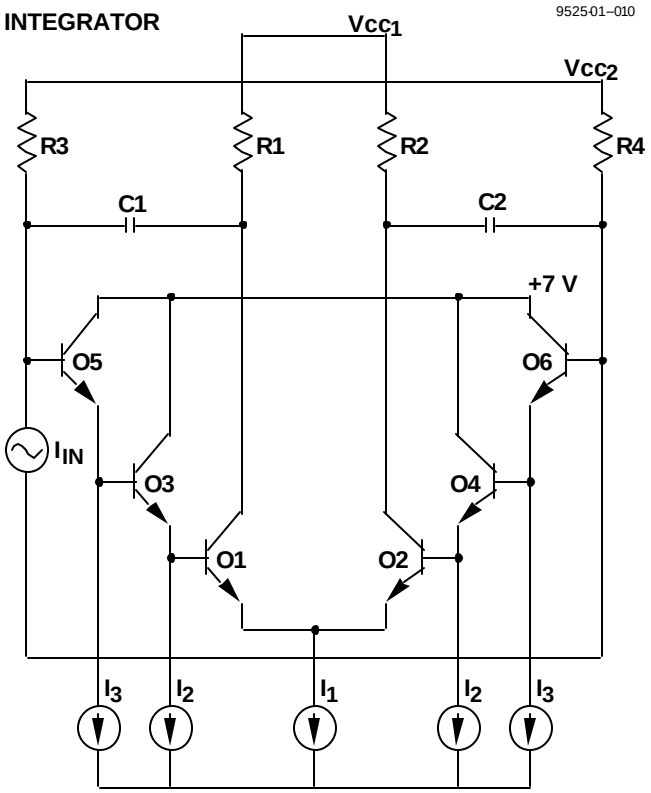
Transconductance Cell Saturation Characteristic

Converts differential input voltage to a differential current signal
Over all ADC linearity and distortion determined by the performance of this circuit



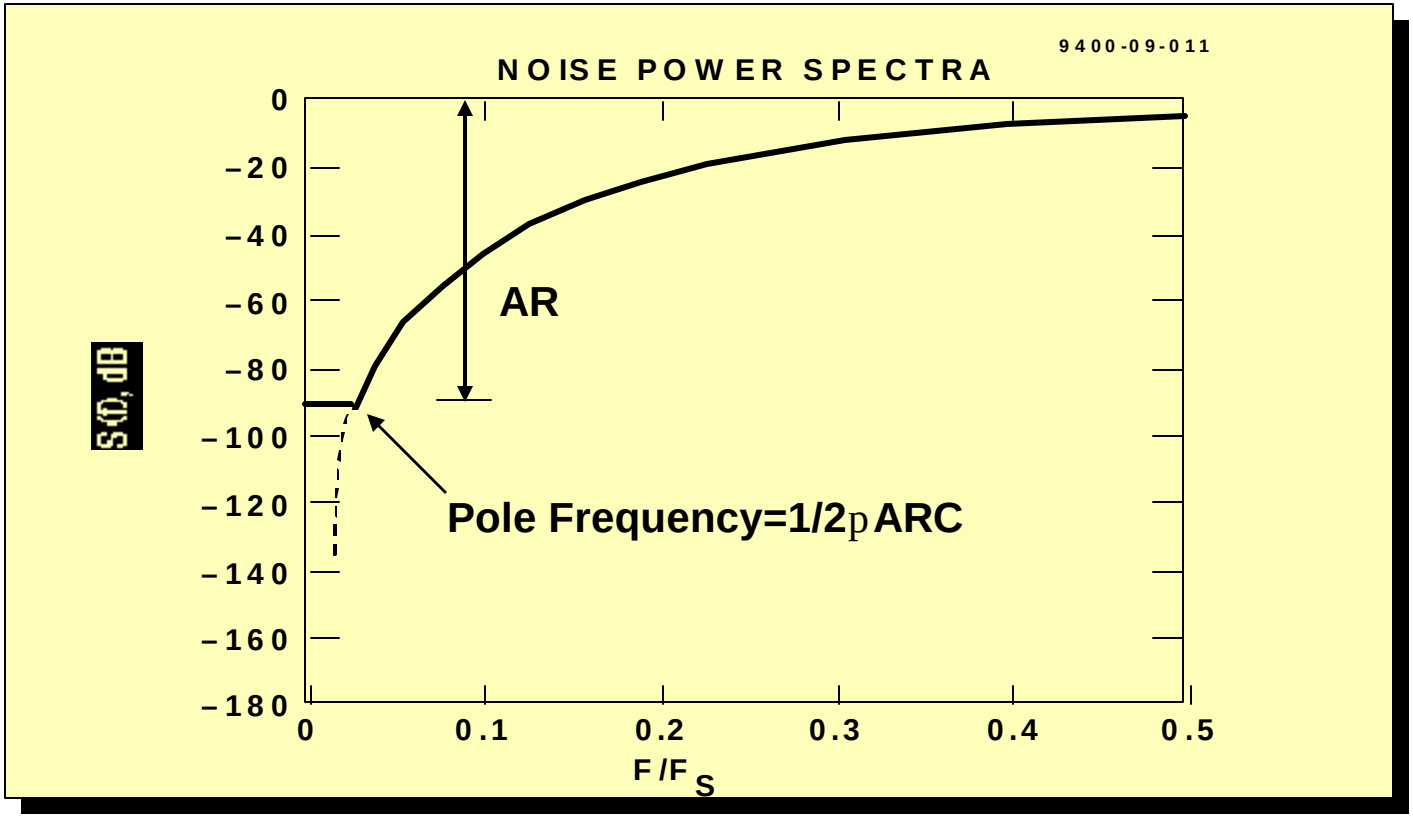


Integrator Design



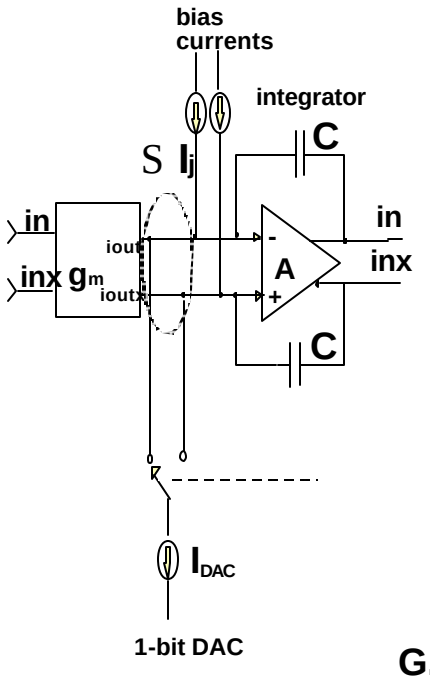
- **Differential amplifier with gain, A and feedback capacitors, C**
- **Low frequency gain determines the noise floor of DS modulator near DC**
- **Low frequency gain limited by ARC, where R is the effective resistance as seen at the current summing node**

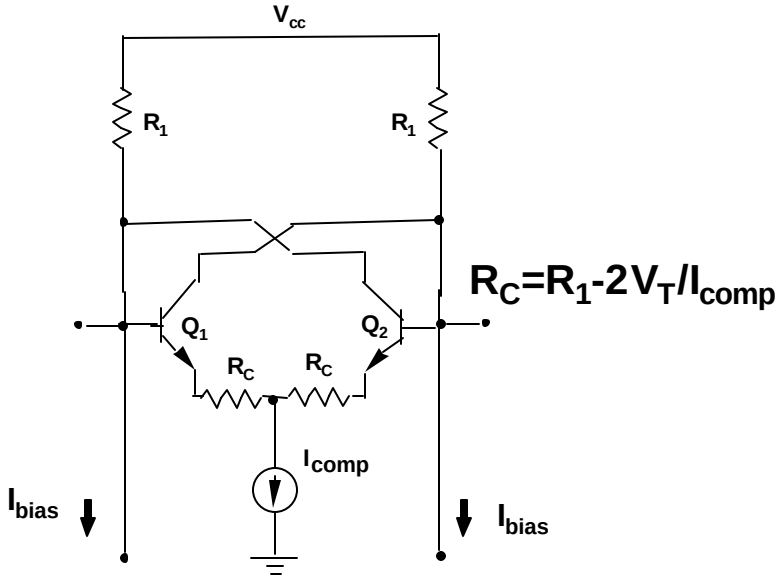
Finite Tranimpedance Gain Limits Noise Floor



Positive Current Source

Positive current source needs to supply the current for the Gm cell and DAC
The effective resistance of the positive current source determines the overall transimpedance gain (ARC)

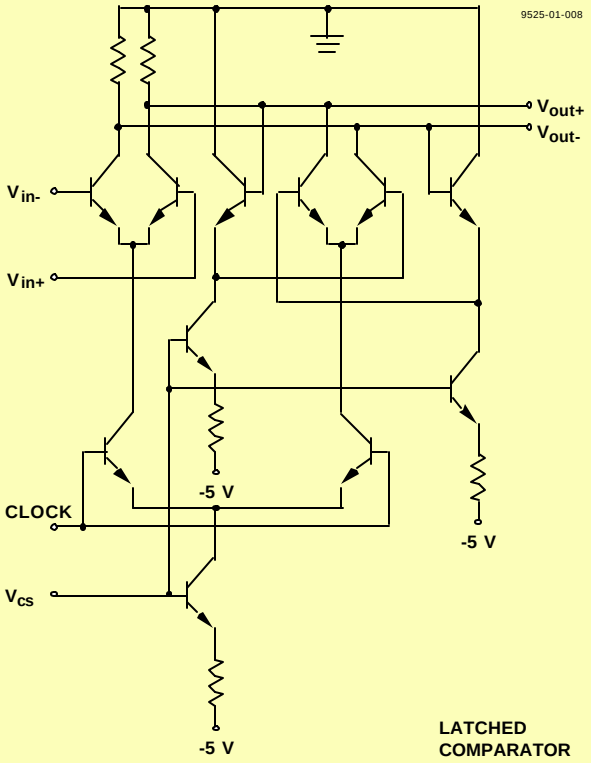




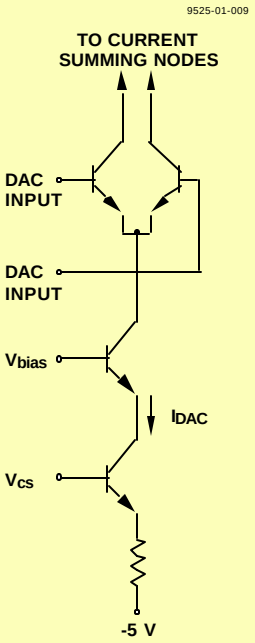
$R_{eff}=V_A/2I_{bias}$

G.A. De Veirman, et.al. JSSC Vol 27, No. 3, March 1992, pp 324-331

Comparator and DAC Cells



LATCHED COMPARATOR

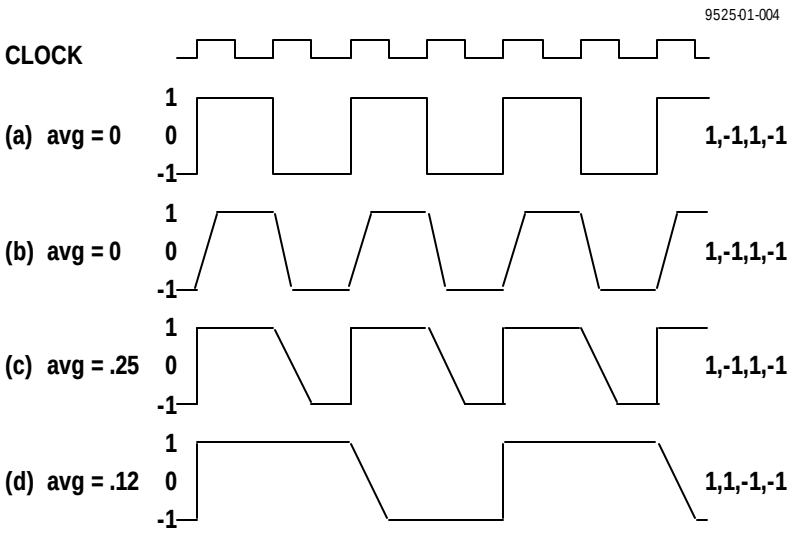


ONE BIT DAC

Non-return to zero DAC

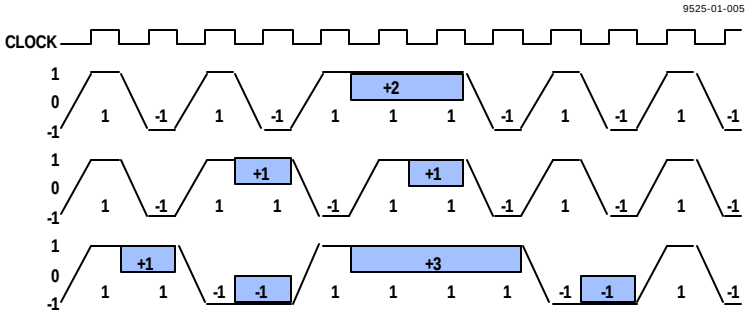
Asymmetric Rise and Fall Times

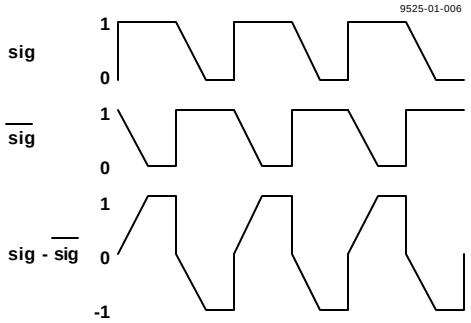
Asymmetric Rise and Fall Times Produce a Signal Dependent Distortion



- Ideal DAC waveform: average value of alternating sequence is zero
- Equal nonzero rise and fall times: average value of an alternating sequence is zero
- Asymmetric rise and fall times: alternating single pulses dc value not equal to zero
- Asymmetric rise and fall: alternating pairs of pules has dc value different from alternating single pules

Symmetric Rise and Fall Times



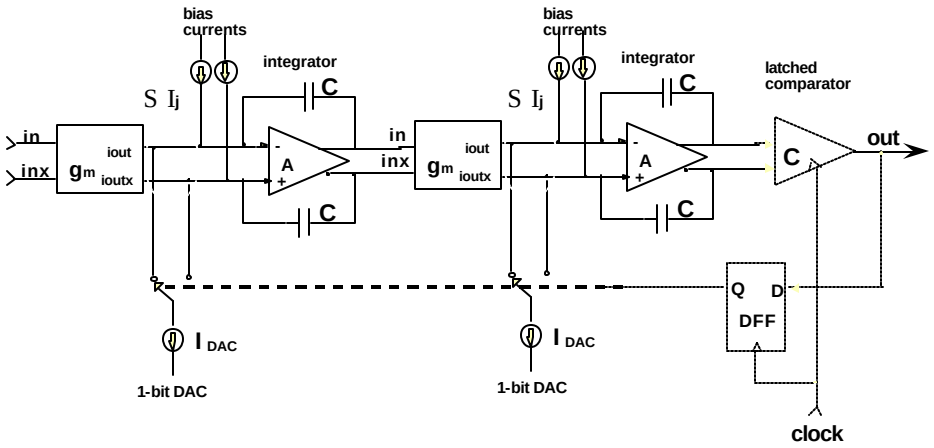


- **Symmetric finite rise and fall times do not effect the integrated area of the pulse train**

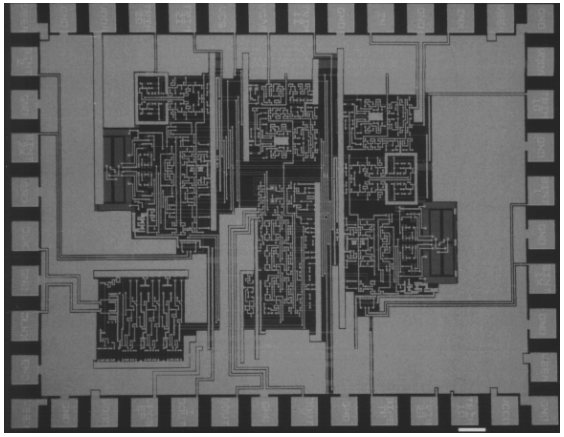
- **Balanced differential signals are inherently symmetric even if the individual components are asymmetric**

InP HBT 2nd Order ΔΣ Modulator

Block Diagram



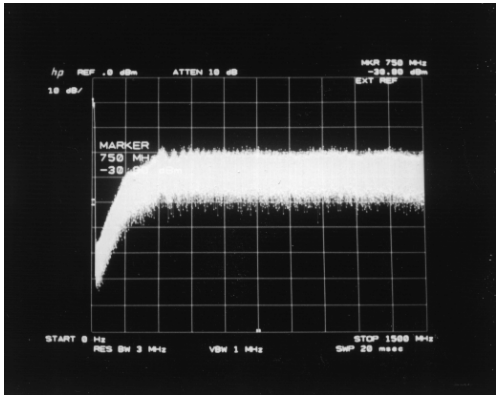
Die Photo



2nd Order ΔΣ Modulator
2.0 mm x 1.5 mm Die Size
250 HBTs

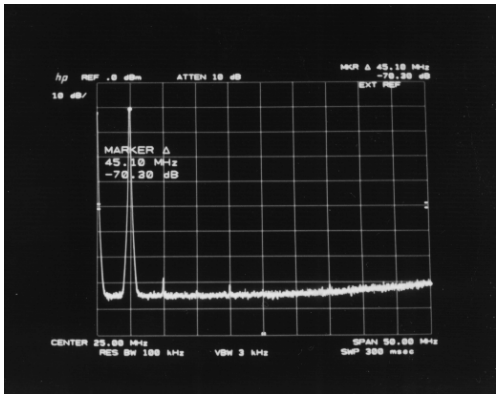
3.2 GHz Sample Rate

9525-01-013



ΔΣ **Output Spectrum (0 to 1.5 GHz)**

9525-01-014



SFDR=
70 dB

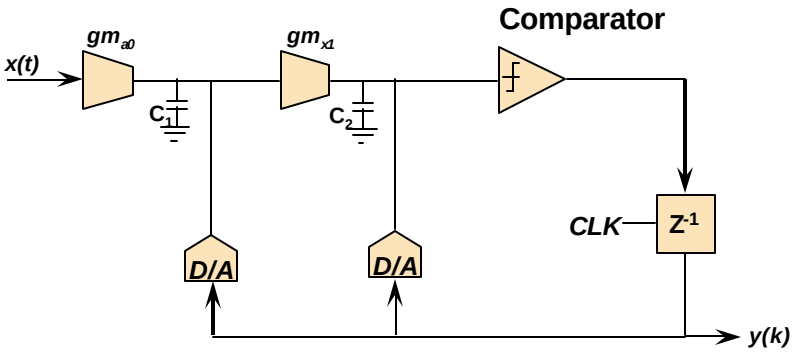
Signal Band for 100 MSPS ADC

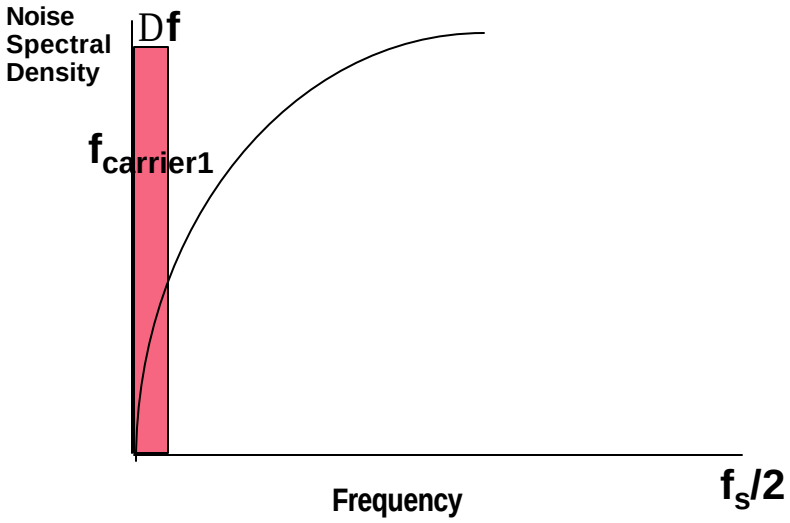
Joe Jensen
(310) 317-5250
jfjensen@hrl.com

slide #17

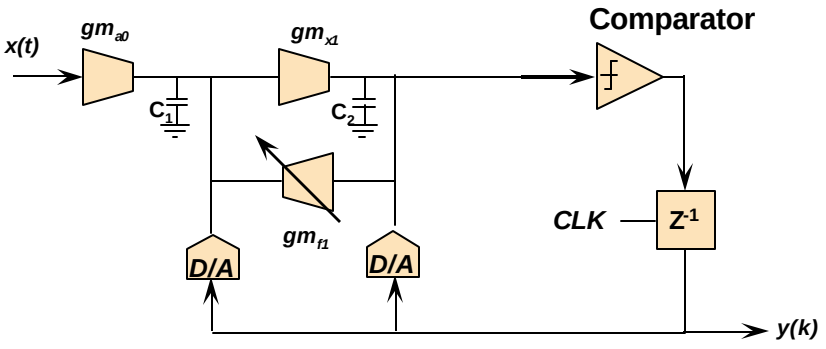
Conversion of Low Pass ΔΣ Modulator to Bandpass ΔΣ Modulator

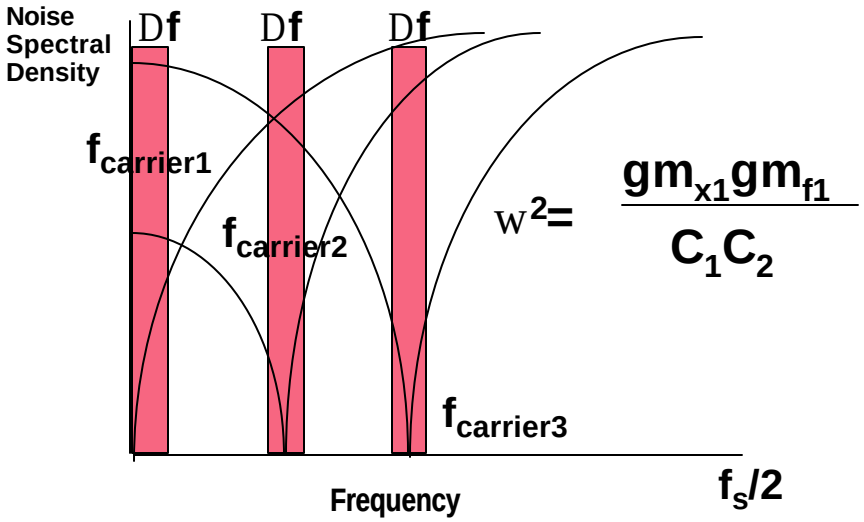
Low Pass





Bandpass

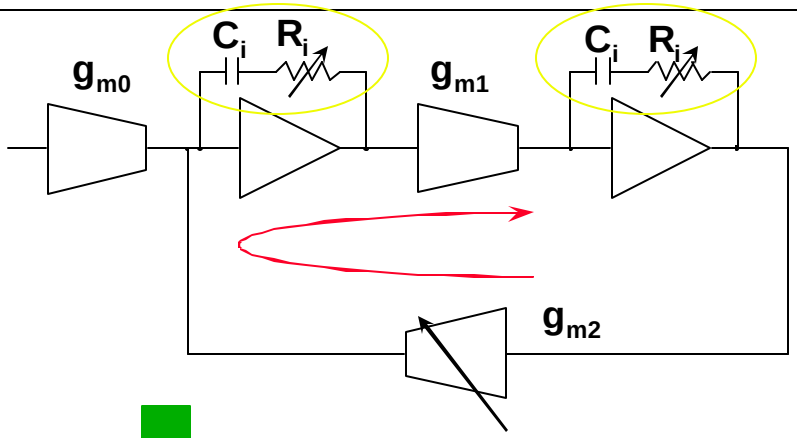




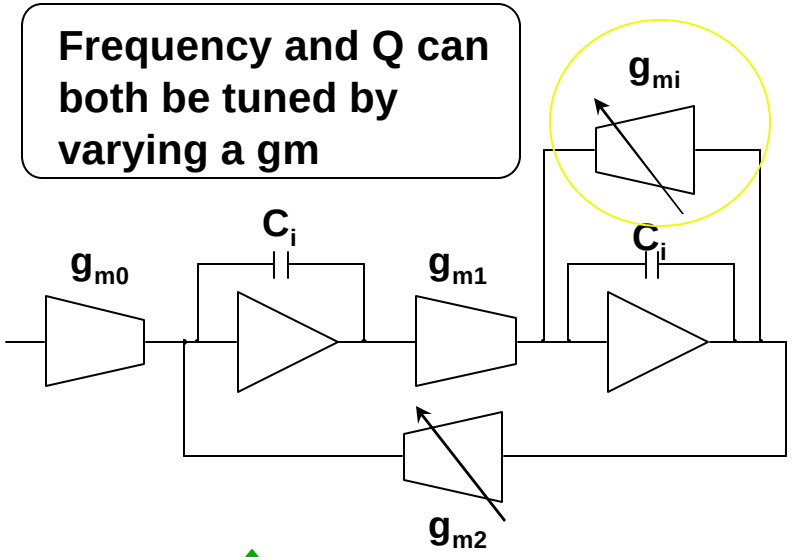
Joe Jensen
(310) 317-5250
jfjensen@hrl.com

Resonator Sensitivity to Interconnect Delay - Q-Tuning Circuit

Lead-lag network required for 180° phase.

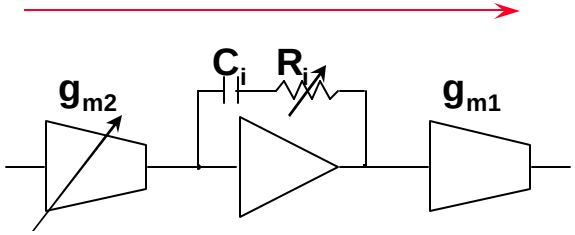


Frequency and Q can both be tuned by varying a gm

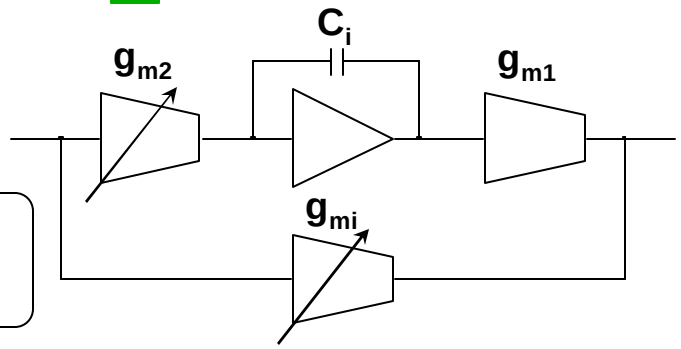


Redraw resonator

Resonator response is sensitive to R_i. Need tunability

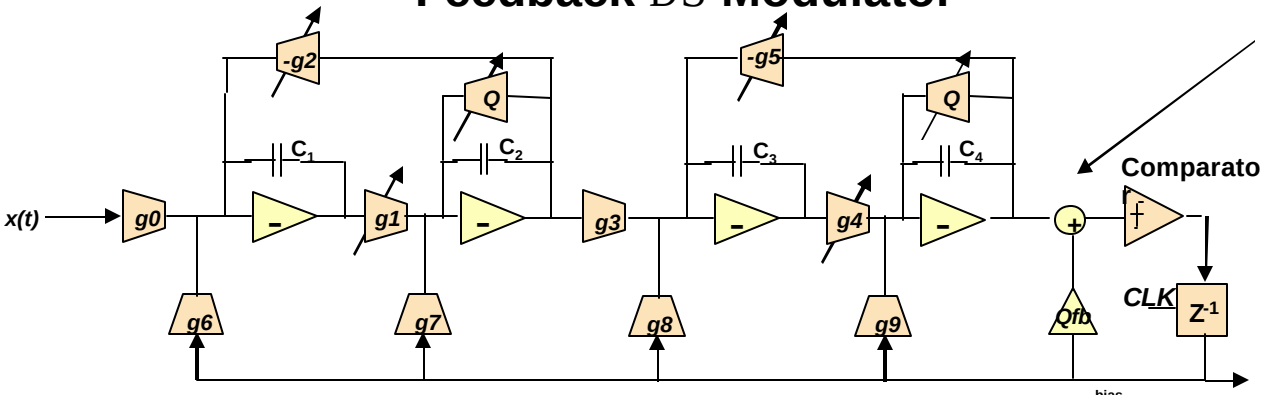


Equivalent circuits if: $gm_i = gm_1gm_2R_i$

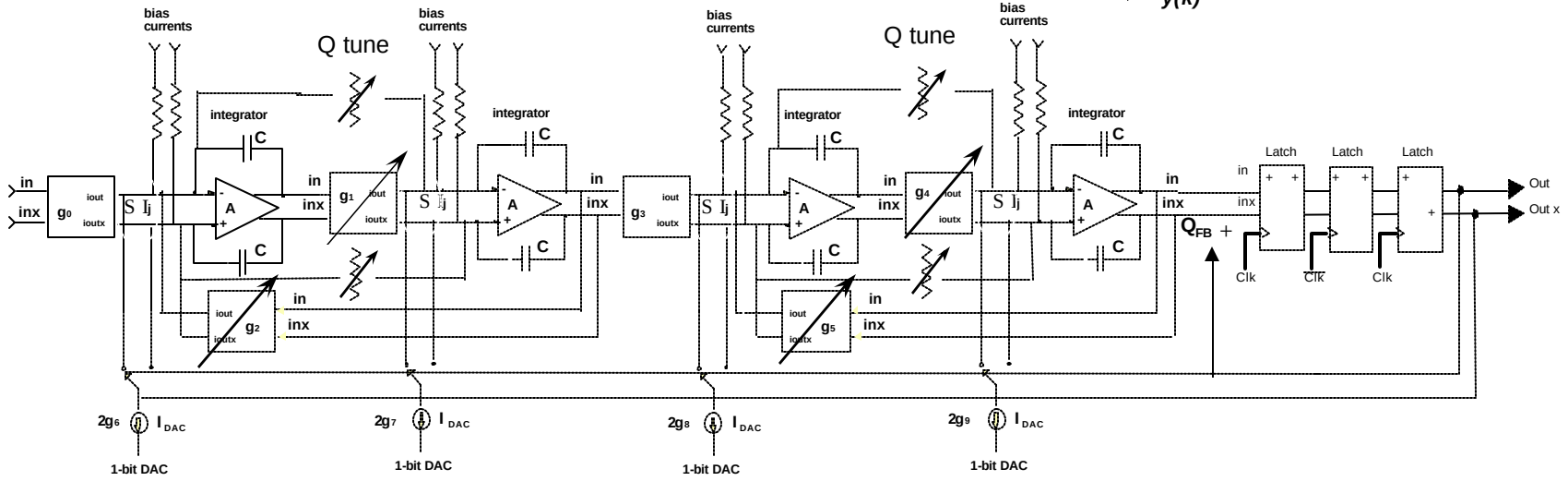


4th Order Bandpass DS Modulator Continuous Time Architecture

Feedback DS Modulator



- Qfb reduces signal delay
  - Improves stability
  - Improves wideband SNR
  - Improves gain flatness



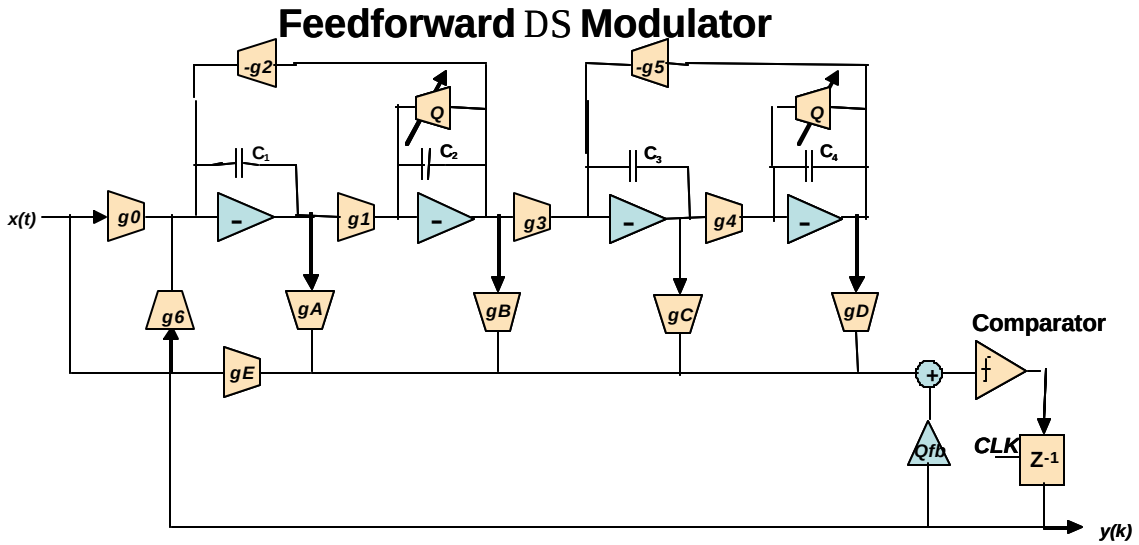
Q-tuning eliminates need for positive current source

- Q feedback cancels finite impedance of pull up resistors

Feedforward Architecture

Advantages of Feedforward Architecture

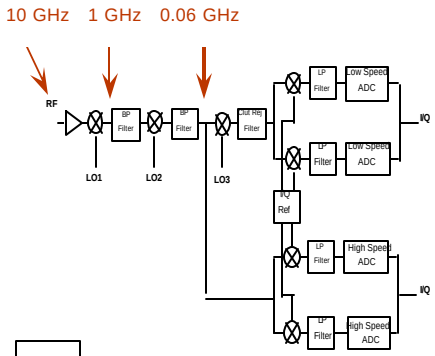
- Only one feedback DAC is required to be fed to the noise-shaping loop
- Less harmonic distortion ??? *Better IMD*
- Less sensitive to circuit imperfection
- Can handle more input signal power
  - *Better saturation recovery response*



InP HBT IF Bandpass DS Modulator
4th Order, 1-Bit DS, 4 GSPS, 2nd IF Sampling

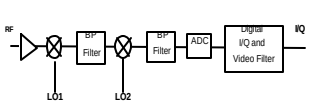
*** Published JSSC Oct. 2004**

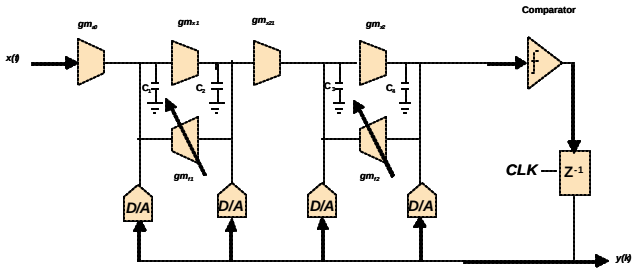
Conventional Analog I/Q Receiver



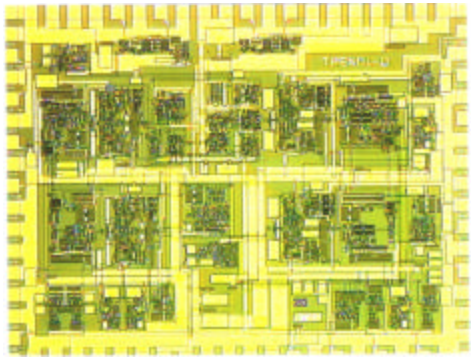
Enhanced Performance
Lower Power
Lower Size & Weight
Lower Cost

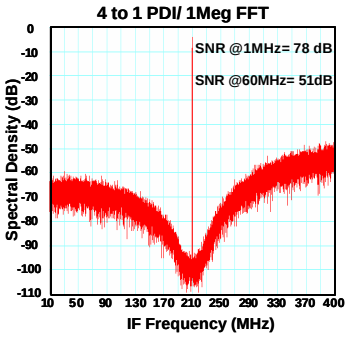
IF Sampling Receiver

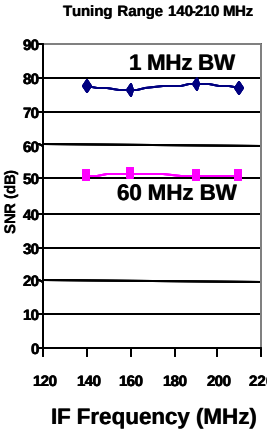


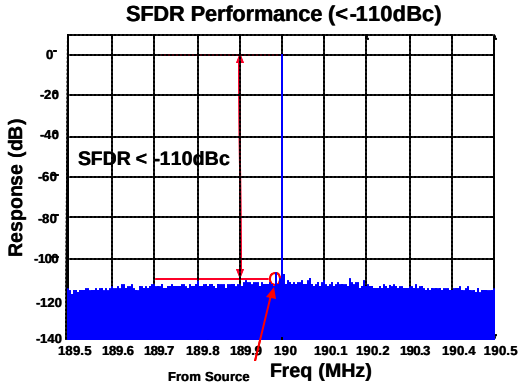


4th order, tunable IF, bandpass DS Modulator



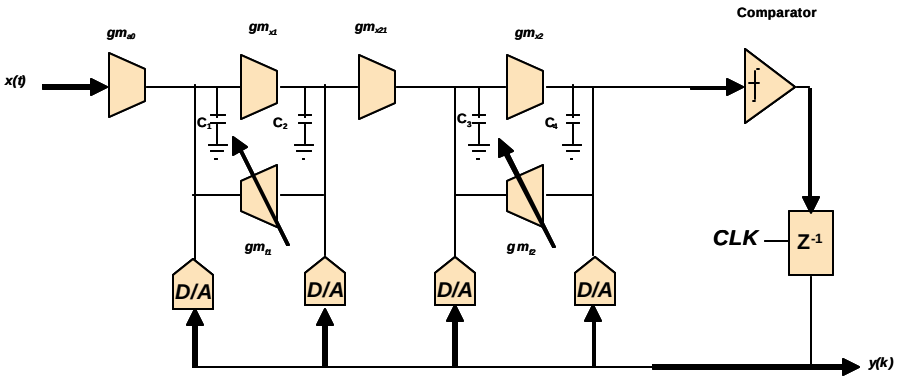






Passive versus Active Gm-C Resonators

Active GM-C 4th Order



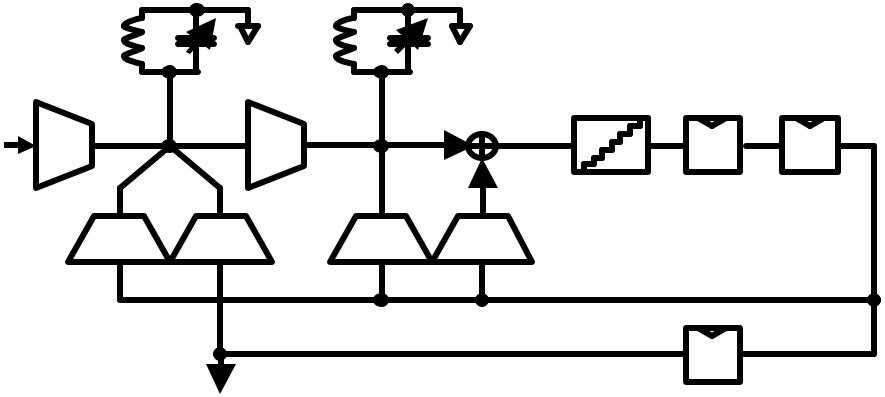
Advantages

- Small size for lower frequencies
- Electronically Tunable

Disadvantages

- Higher noise figure
- Low Linearity
- Higher Power Dissipation
- Frequency range limited to < $f_T/20$

Passsive L-C 4th Order



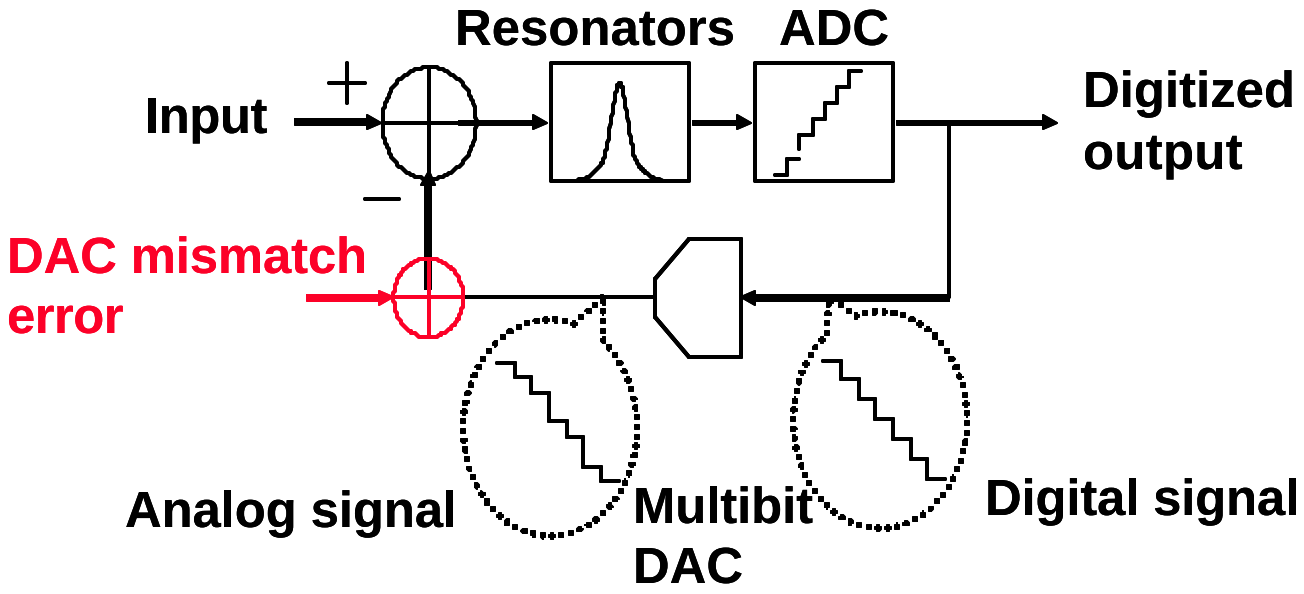
Advantages

- Lower Noise Figure
- High Linearity
- Higher Frequency Operation
- Lower Power

Disadvantages

- Harder to electronically tune
- Large size for low frequencies < 500 MHz

Multi-bit ΔΣ Modulators



Advantages

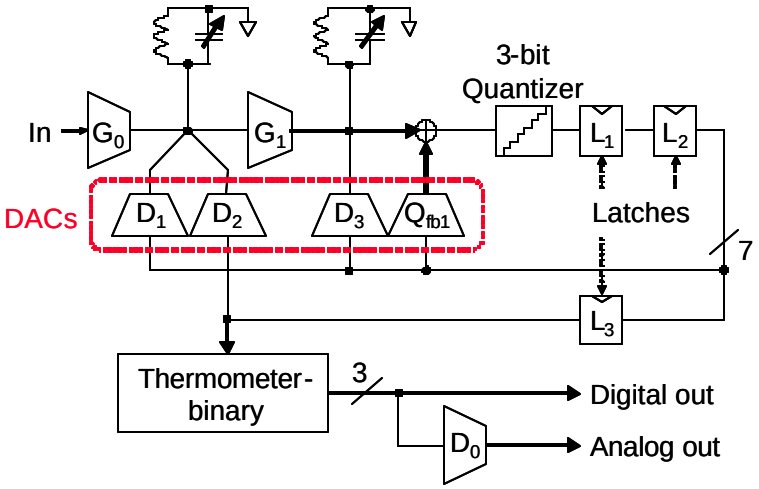
- High resolution over wider bandwidth
- Increased stability for high order ΔΣ modulators
- Reduced sensitivity to DAC timing errors

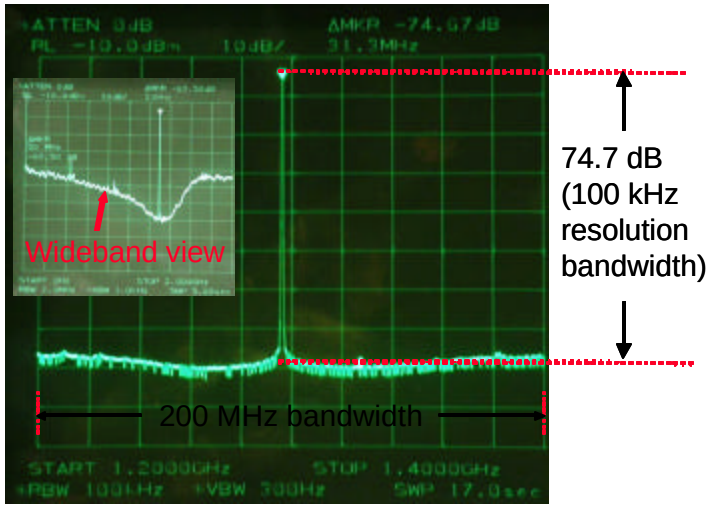
Disadvantage

- Resolution limited by multi-bit DACs element mismatch and linearity

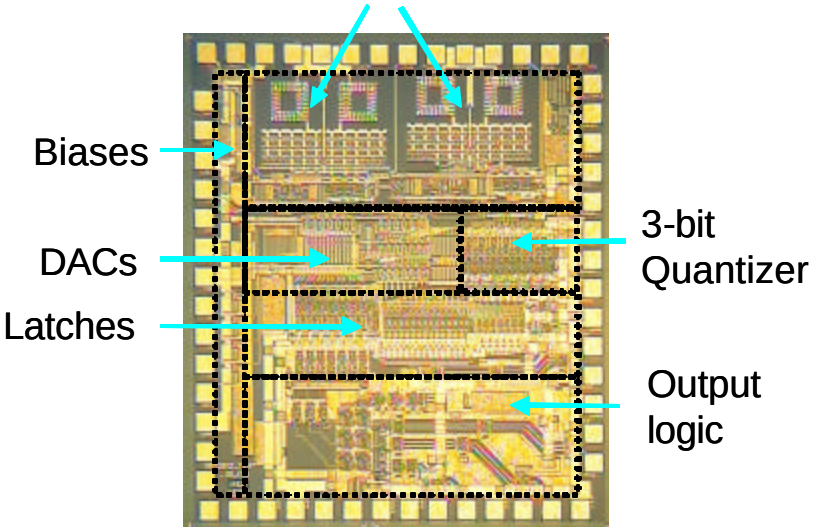
InP HBT 1st IF Bandpass ΔΣ 4th Order, 3-Bit, 4GSPS, 1.4GHz IF Sampling

*** Published CICC 2003**

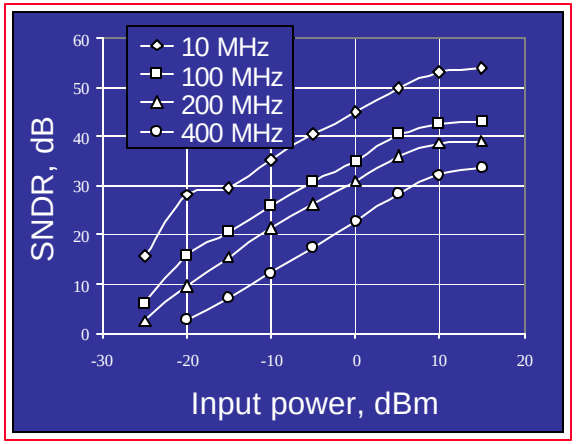




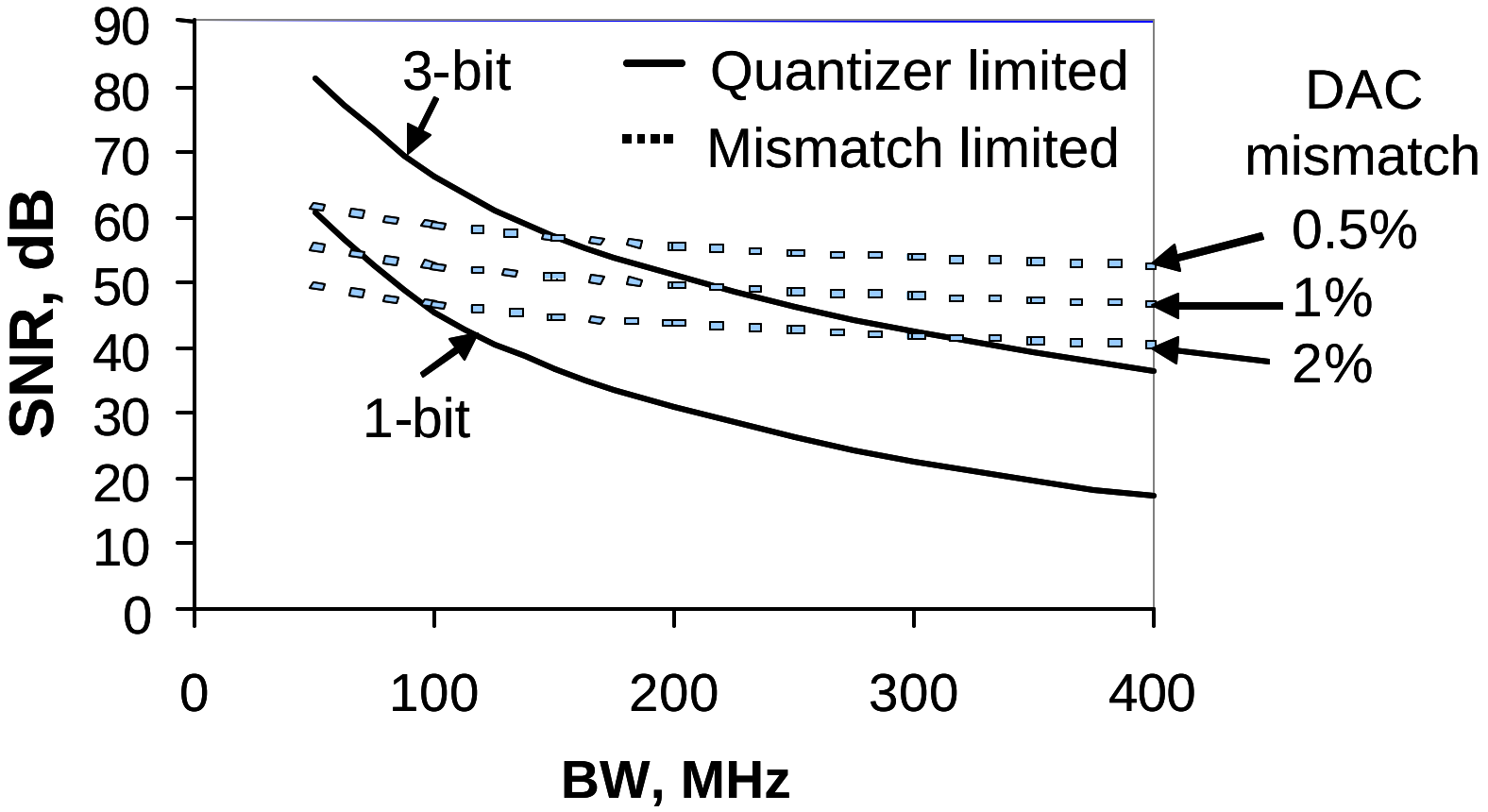
Resonators and G_m-cells



Q-tuned internal LC resonators (Q ~= 10)
No mismatch shaper

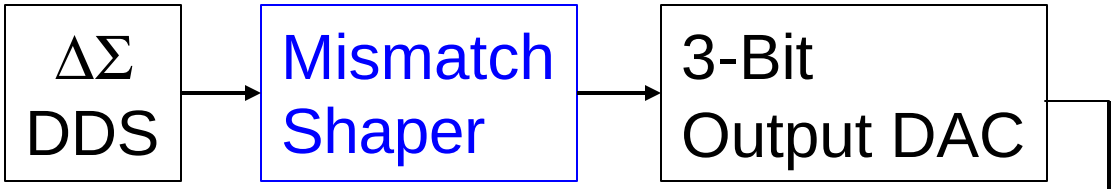


Multibit DAC Mismatch Errors

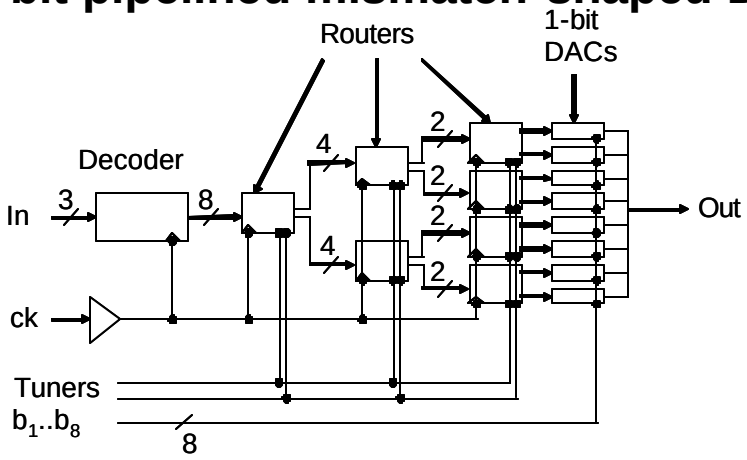


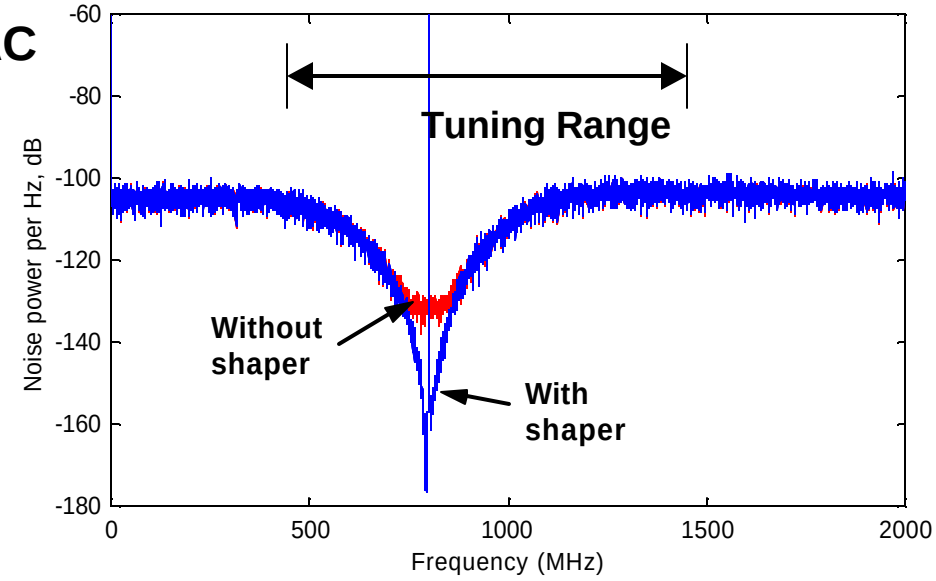
DAC Mismatch Shaping

- **Moves DAC mismatch errors away from signal**
- **Eliminates spurs caused by DAC mismatches**
- **Enables high resolution signal generation using a multi-bit DAC**



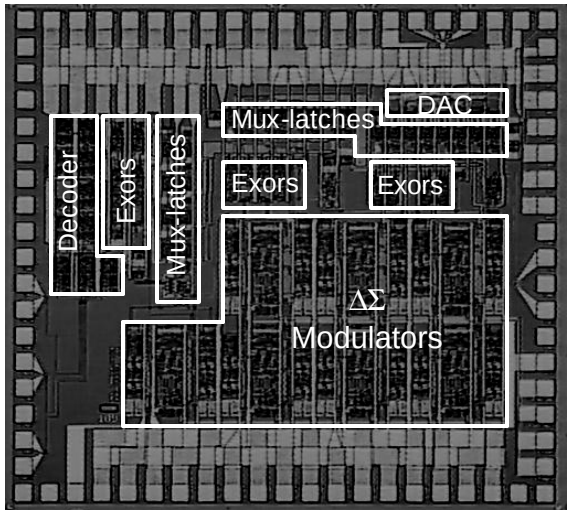
3-bit pipelined mismatch-shaped DAC

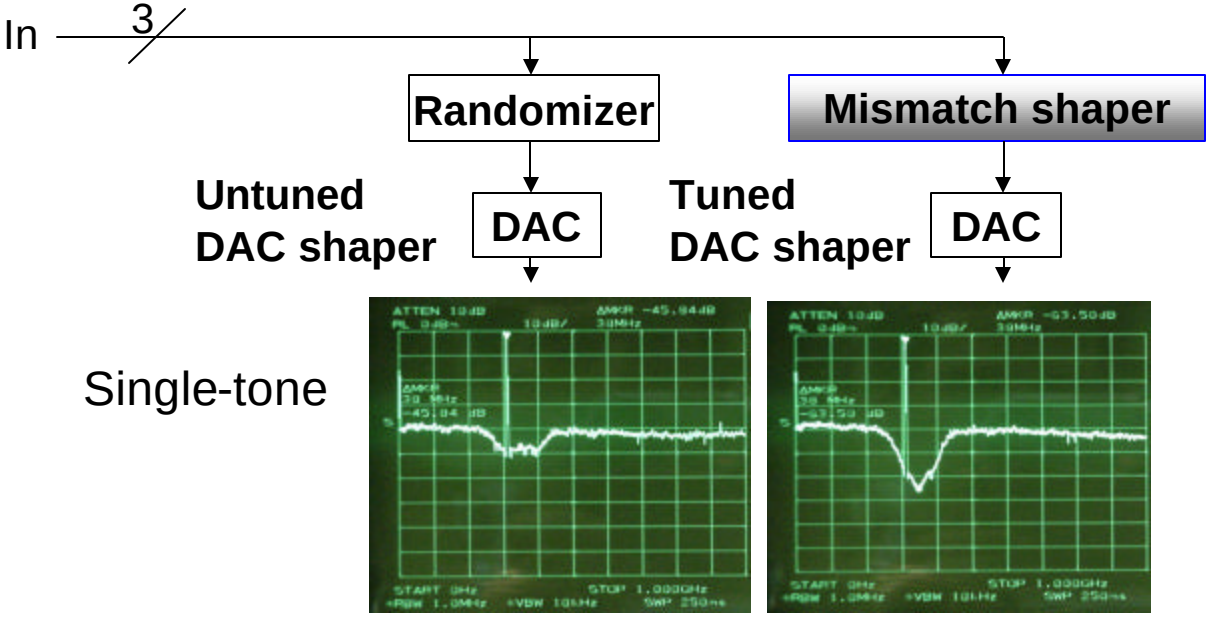




3-bit, 2 GS/s ΔΣ DAC with Tunable Mismatch Shaper

*Published ISSCC 2004

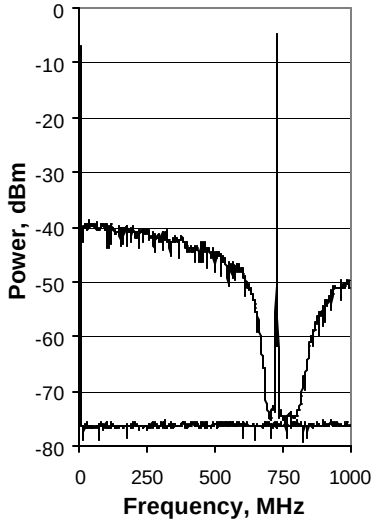




10-20 dB improvement in SNR and IMD from mismatch shaping

SNR > 68 dB/1 MHz BW from 250-750 MHz IF

IMD <-80 dBc from 250-750 MHz IF



Conclusions

- **Bandpass DS modulation is an ideal ADC architecture for digital receivers**
  - **Elimination of downconversion stages and analog IF filters**
  - **Improved I and Q matching**
  - **Improved performance with digital modulaton schemes**
  - **Improved flexibility with communication standards**
  - **Reduction of size, weight, power, and cost for multimode receivers**